

CLAIMS

I claim:

1. A method for changing a configuring of an error correction code (ECC) logic circuit for performing an error-check of a changed data-width comprising:

sequentially interconnecting a set of N1 identical error-check blocks where N1 is a first positive integer; and

reconfiguring said ECC logic circuit by changing said ECC logic circuit to a set of N2 sequentially interconnected circuits comprising N2 of said identical error-check blocks where N2 is a second positive number.

2. The method of claim 1 wherein:

said step of sequentially interconnecting a set of N1 identical error-check blocks is a step of interconnecting said N1 error-check blocks only between sequentially neighboring blocks for transmitting signals only between said neighboring error-check blocks; and

said step of reconfiguring said ECC logic circuit by changing said ECC logic circuit to a set of N2 sequentially interconnected circuits is a step of interconnecting said N2 error-check blocks only between sequentially neighboring blocks for transmitting signals only between said neighboring error-check blocks.

3. A method for operating a memory device comprising a plurality of memory cells, comprising:

performing an error-check on said memory cells; and

repairing a faulty memory cell storing an error data bit.

4. The method of claim 3 wherein:

said step of repairing a faulty memory cell further  
comprising a step of performing said step of repairing said  
faulty memory cell automatically by writing a correct bit into  
said faulty memory cell.

5. A memory device comprising a plurality of memory cells  
each having a floating gate for storing a plurality of electric charges  
therein, said memory device further comprising:

an error-check logic circuit includes a set of identical error-  
check blocks sequentially interconnected for checking errors  
of data storage in said memory cells.

6. The memory device of claim 5 further comprising:

a multiple-level voltage means for applying at least two  
electrical charge levels on said floating gates for representing  
at least two binary bits stored in said memory cells.

7. The memory device of claim 6 further comprising:

a multiple-level electrical-charge sensing means for sensing  
at least two electric-charge levels stored in said floating gates  
for detecting at least two binary bits stored in said memory  
cells.

8. The memory device of claim 7 wherein:

said multiple-level electrical-charge sensing means further  
comprising a bit-pattern means for generating a bit-pattern  
based on said electric-charge levels sensed by said multiple-  
level electrical-charge sensing means.

9. The memory device of claim 7 wherein:

5 said bit-pattern means is further provided for generating a sequence of bit-patterns based on said electric-charge levels wherein each of said bit patterns based on a first electrical-charge level differing by only a single bit from a second bit-pattern representing a second electrical-charge level sequentially adjacent to said first electrical-charge level.

10 10. A memory device comprising a plurality of memory cells each having at least two memory-cell characteristic-states each representing a bit-pattern stored therein, said memory device further comprising:

15 an error-check logic circuit includes a set of identical error-check blocks sequentially interconnected for checking errors of data storage in said memory cells.

20 11. A content addressable memory (CAM) device comprising a plurality of memory-cell arrays for storing an array content therein provided for an data-access to an array based on a match with said array content, said CAM device further comprising:

25 an error-check logic circuit for checking errors of said data access to each of said memory-cell arrays.

12. The content addressable memory (CAM) device of claim 11 further comprising:

30 an error-code storage means for storing an error-code check (ECC) bit for each of said memory-cell array used by said error-check logic circuit for checking errors of said data access to each of said memory-cell arrays.

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13. The content addressable memory (CAM) device of claim 11  
wherein:

each of said memory-cell array further storing an error-code  
check (ECC) bit generated by said error-check logic circuit  
for checking errors of said data access to each of said  
memory-cell arrays.

14. The content addressable memory (CAM) device of claim 11  
wherein:

said error-code storage means is a random access memory  
(RAM) device for storing said error-code check (ECC) bit for  
each of said memory-cell array used by said error-check  
logic circuit for checking errors of said data access to each of  
said memory-cell arrays.

15. A memory device comprising a plurality of memory cells  
each having a floating gate for storing a plurality of electric charges  
therein, said memory device further comprising:

a multiple-level electrical-charge sensing means for sensing  
at least two electric-charge levels stored in said floating gates  
as a sequence of charge levels for detecting at least two  
binary bits for recording a plurality of bit patterns stored in  
said memory cells;

said multiple-level electrical-charge sensing means further  
includes a bit-pattern means for generating a sequence of  
bit-patterns based on said sequence of electric-charge levels  
wherein each of said bit patterns based on a first electrical-  
charge level differing by only a single bit from a second bit-  
pattern represented by a second electrical-charge level  
sequentially adjacent to said first electrical-charge level.

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